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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/886,776      | 06/21/2001  | Sunetra K. Mendis    | JCLA6195            | 6128             |

7590 10/22/2004

J C Patents Inc  
4 Venture Suite 250  
Irvine, CA 92618

EXAMINER

VILLECCO, JOHN M

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2612

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                               |                               |  |
|------------------------------|-------------------------------|-------------------------------|--|
| <b>Office Action Summary</b> | Application No.<br>09/886,776 | Applicant(s)<br>MENDIS ET AL. |  |
|                              | Examiner<br>John M. Villecco  | Art Unit<br>2612              |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-9,13 and 15-19 is/are rejected.
- 7) ☒ Claim(s) 4,10-12,14 and 20-22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.                                                |

## **DETAILED ACTION**

### ***Specification***

1. The disclosure is objected to because of the following informalities:
  - On page 6, line 13, applicant refers to the reset transistor as reference number 40. It is clear from Figure 1 and the previous comments in the specification that the correct reference number for the reset transistor is 20.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
3. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
4. Regarding claim 2, applicant recites the limitation of “using a hard or soft reset dependent on signal level”. It is unclear from the claim what signal level is being discussed. There are several different signals discussed in the specification and it is unclear what signal is being referenced. Applicant discusses several signals including and image signal level, a reset signal level, and gain signals. For examination purposes it will be assume that the applicant is referring to the level of the gain signals gr, gg, and gb, as discussed on page 7, lines 17-20.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1, 3, and 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Pain et al. (U.S. Patent No. 6,721,464).**

7. Regarding *claim 1*, Pain discloses a CMOS imager capable of controlling image lag at low light levels by controlling a reset level. The HTS pixel (1150) is capable of performing a hard reset and then a soft reset in order to reduce image lag. See column 3, lines 7-10 and column 6, line 44 to column 7, line 25.

8. As for *claim 3*, Pain discloses a pixel structure which includes a photodiode (SENSE) node (702) for acquiring image data, a reset transistor (706), a readout transistor (no reference number in Figure 7), and a selection transistor (SEL) for selecting the pixel to be read out. \The HTS pixel (1150) is capable of performing a hard reset and then a soft reset in order to reduce image lag. See column 3, lines 7-10 and column 6, line 44 to column 7, line 25.

9. With regard to *claim 5*, as mentioned above in the discussion of claim 3, Pain discloses that the imaging device is a photodiode.

10. Regarding *claim 6*, each of the transistors used in the pixel of Figure 7 and 11B are the same type of transistor.

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11. As for *claim 7*, Pain discloses that the reset level is independent of the photosignal strength (col. 7, lines 16-25). The photosignal strength is interpreted to be a preceding signal level.

12. **Claims 3, 5-9, 13, and 15-19 rejected under 35 U.S.C. 102(e) as being anticipated by Zhao et al. (U.S. Patent No. 6,727,946).**

13. *Claim 3* can also be rejected based upon Zhao. Zhao discloses a sensor (S1) for acquiring image data, a reset transistor (RST), a buffer transistor (M2) which acts as the readout transistor, and a selection transistor (M3). By controlling which reset signal ( $V_H$  or  $V_L$ ) is applied to the circuit the image lag is reduced.

14. *Claim 5* can also be rejected based upon Zhao. Zhao discloses that the sensor (S1) can be a photodiode. See column 7, line 34.

15. *Claim 6* can also be rejected based upon Zhao. Zhao implies in column 4, lines 38-43 that the transistors are all of the same, but can be different if the circuit designer so chooses.

16. *Claim 7* can also be rejected based upon Zhao. Zhao discloses that the reset voltage can be driven to ground before the soft reset takes place. Thus the reset level would be independent of the preceding signal level.

17. With regard to *claim 8*, Pain discloses that the hard reset is defined as a supply voltage ( $V_{dd}$ ) minus the threshold voltage ( $V_T$ ). See column 2, lines 41-65.

18. As for *claim 9*, Pain discloses a specific embodiment of the invention in which the  $V_H$  is set to the supply voltage ( $V_{DD}$ ) and  $V_L$  is ideally set to  $V_{DD}$  minus the threshold voltage ( $V_T$ ) (see equation 7). The voltage line is switched between  $V_H$  and  $V_L$ .

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19. Regarding **claim 13**, Zhao discloses a sensor (S1) for acquiring image data, a reset transistor (RST), a buffer transistor (M2) which acts as the readout transistor, and a selection transistor (M3). Pain discloses a specific embodiment of the invention in which the  $V_H$  is set to the supply voltage ( $V_{DD}$ ) and  $V_L$  is ideally set to  $V_{DD}$  minus the threshold voltage ( $V_T$ ) (see equation 7). The voltage line is switched between  $V_H$  and  $V_L$ . By controlling which reset signal ( $V_H$  or  $V_L$ ) is applied to the circuit the image lag is reduced.

20. With regard to **claim 15**, Zhao discloses that the sensor (S1) can be a photodiode. See column 7, line 34.

21. As for **claim 16**, Zhao implies in column 4, lines 38-43 that the transistors are all of the same, but can be different if the circuit designer so chooses.

22. Regarding **claim 17**, Zhao discloses that the reset voltage can be driven to ground before the soft reset takes place. Thus the reset level would be independent of the preceding signal level.

23. With regard to **claim 18**, Pain discloses that the hard reset is defined as a supply voltage ( $V_{dd}$ ) minus the threshold voltage ( $V_T$ ). See column 2, lines 41-65 and equation 7.

24. As for **claim 19**, Pain discloses a specific embodiment of the invention in which the  $V_H$  is set to the supply voltage ( $V_{DD}$ ) and  $V_L$  is ideally set to  $V_{DD}$  minus the threshold voltage ( $V_T$ ) (see equation 7). The voltage line is switched between  $V_H$  and  $V_L$ .

***Allowable Subject Matter***

25. Claim 2 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

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26. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 2, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest improving image quality at low light levels by using hard or soft reset dependent upon the gain signal levels.

27. Claims 4, 10-12, 14, and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. The following is a statement of reasons for the indication of allowable subject matter:

Regarding *claims 4 and 14*, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that an amplifier gain setting is used to determine whether to use a hard reset or a soft reset.

As for *claims 10 and 20*, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the reset drain level is determined by using gain of one color of pixel.

With regard to *claim 11 and 21*, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the reset drain level is determined by using a middle gain.

Regarding *claims 12 and 22*, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the reset drain level is changed only when gains of all color pixels satisfy threshold conditions.

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Any response to this action should be mailed to:

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

or faxed to:

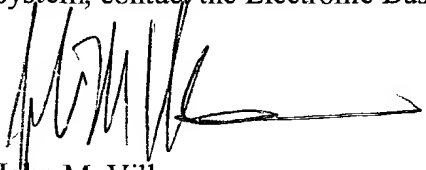
(703) 872-9306 (For either formal or informal communications intended for entry. For informal or draft communications, please label **"PROPOSED"** or **"DRAFT"**)

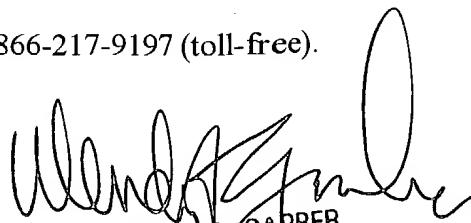
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington VA, Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (703) 305-1460. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
John M. Villecco  
October 6, 2004

  
WENDY R. GARBER  
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TECHNOLOGY CENTER 2600